06-12-00

PATENT
Docket No. P1057

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: ROBERT B.OGLE, JR.
MARINA V. PLAT
MARK T. RAMSBEY

SERIAL NO.: FILED HEREWITH EXAMINER: UNASSIGNED

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FOR: ANTI-REFLECTIVE INTERPOLY DIELECTRIC

BOX PATENT APPLICATION
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TRANSMITTAL LETTER

Dear Sir:

In connection with the above-referenced patent application, transmitted herewith are the following:

1. Specification (4 pages), Claims (3 pages), and Abstract (1page);
2. Formal Drawings (1 sheet, 2 figures);
3. Declaration and Power for Patent Application (2 pages);
4. Assignment Agreement (3 pages);
5. Recordation Form Sheet Form, PTO-1595 (1 page);
6. Check No. 2865 in the amount of $690.00 for patent application filing fee;

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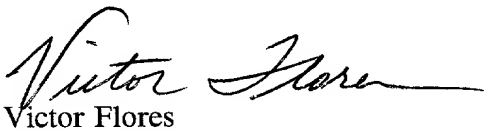

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Patent
Docket No. P1057

PATENT APPLICATION

ANTI-REFLECTIVE INTERPOLY DIELECTRIC

INVENTORS: ROBERT B. OGLE, JR.
MARINA V. PLAT
MARK T. RAMSBEY

RELATED APPLICATION

This application is related to co-pending U. S. Provisional Patent Application Ser. No. 60/179,291, entitled "ANTI- REFLECTIVE INTERPOLY DIELECTRIC," filed January 31, 2000.

TECHNICAL FIELD

The present invention relates to the manufacture of semiconductor devices. More specifically, the present invention relates anti-reflective coatings used in the flash memory semiconductor devices.

BACKGROUND OF THE INVENTION

In the production of semiconductor devices, an anti-reflective coating is used to cut down on light scattering from a surface into a resist mask. By reducing the scattered light, anti-reflective coatings allow for superior patterning and better defining small images. In addition, anti-reflective coatings minimize standing wave effects, such minimization improving the image contrast. In conventional flash memory devices, anti-reflective coatings are placed

on the top of core stacks, where additional processing is required to place the anti-reflective coating on the core stacks. Figure 1 is a cross sectional view of a conventional core stack 10 mounted on a substrate 12 used in prior art flash memory. The core stack 10 comprises a tunnel oxide layer 14 on the substrate 12, a first polysilicon layer 16 formed over the tunnel oxide layer 14, a interpoly layer 18 formed over the first polysilicon layer 16, a second polysilicon layer 20 formed over the interpoly layer 18, and an anti-reflective coating 22 formed over the second polysilicon layer. In the related art, the interpoly layer 18 is made of three layers, which are a first oxide layer 24 on the first polysilicon layer 16, a nitride layer 26 on the first oxide layer 24, and a second oxide layer 28 between the nitride layer 26 and the second polysilicon layer 20 and is called the oxide-nitride-oxide (ONO) layer. The ONO layer forms a dielectric layer, which in the prior art is between about 200 to 300 Å thick. Thus, to obtain the benefits of the anti-reflective coating, without the additional processing steps required for an anti-reflective coating, would be desirable.

BRIEF SUMMARY OF THE INVENTION

It is an object of the invention to provide the benefits of an anti-reflective coating on the core stacks, without the additional processing steps required by an anti-reflective coating. Accordingly, the foregoing objects are accomplished by forming an interpoly dielectric layer that has anti-reflective properties. Other features of the present invention are disclosed or apparent in the section entitled "DETAILED DESCRIPTION OF THE INVENTION."

BRIEF DESCRIPTION OF DRAWINGS

For a fuller understanding of the present invention, the accompanying drawings are below referenced.

Figures 1 is a cross sectional view of a flash memory core stack used in the related art.

Figure 2 is a cross sectional view of a flash memory core stack of a preferred embodiment of the invention.

Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

DETAILED DESCRIPTION OF THE INVENTION AND BEST MODE OF THE INVENTION

Figure 2 is a cross sectional view of a core stack 40 of a flash memory device mounted on a substrate 42 in a preferred embodiment of the invention. The core stack 40 comprises a tunnel oxide layer 44 on the substrate 42, a first polysilicon layer 46 formed over the tunnel oxide layer 44, an anti-reflective interpoly layer 48 formed over the first polysilicon layer 46, and a transmissive second polysilicon layer 50 formed over the anti-reflective interpoly layer 48. In the preferred embodiment of the invention, the anti-reflective interpoly layer 48 is formed by a silicon oxynitride (SiON) layer which is between about 300 to 400 Å thick. In the preferred embodiment of the invention, the transmissive second polysilicon layer 50 may be made of either polysilicon on amorphous silicon.

In operation, a photoresist layer 52 is placed over the substrate 42 and core stack 40. A light source with a wavelenghth λ_1 is applied to the resist, where the resist reacts to light with a wavelength λ_1. The polysilicon or amorphous silicon of the transmissive second polysilicon layer 50 is largely transparent to light of the wavelength λ_1 allowing the light to pass through the transmissive second polysilicon layer 50 to the anti-reflective interpoly layer 48. The anti-reflective interpoly layer 48 has an index of refraction n. Using the equation for anti-reflective coatings:

$$2dn=(m+\frac{1}{2})\lambda \qquad m=0,1,2...$$

where d is the thickness of the coating, and where m is the integer number of wavelengths. The equation for the thickness of the anti-reflective interpoly layer 48 is then:

$$d=\frac{(m+\frac{1}{2})\lambda_1}{2n}.$$

For $m = 0$,

$$d=\frac{\lambda_1}{4n}.$$

With film thickness d and index of refraction n meeting the above equation, light of wavelength λ_1 is transmitted through the transmissive second polysilicon layer 50 to the anti-reflective interpoly layer 48. For light of wavelength λ_1, the anti-reflective interpoly layer 48 may be tailored in its thickness d and its index of refraction n to minimize reflection, as is claimed in the present invention. The anti-reflective interpoly layer 48 reduces the amount of light that is reflected, thus allowing for a more detailed imaging of the photoresist layer 52. The photoresist layer 52 is then etched to open apertures in the photoresist layer 52 above source regions and drain regions. A dopant is then implanted to form the source regions 54 and drain regions 56. In use as a flash memory, the anti-reflective interpoly layer 48 has the proper dielectric constant K value to allow the anti-reflective interpoly layer 48 to act as the interpoly layer of a flash memory stack.

Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims. Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

CLAIMS

What is claimed:

1. A flash memory device, comprising:
   a. a substrate;
   b. a plurality of core stacks, wherein each core stack comprises:
      (1) a tunnel oxide layer on the substrate;
      (2) a first polysilicon layer on the tunnel oxide layer;
      (3) an anti-reflective interpoly layer on the first polysilicon layer; and
      (4) a transmissive second polysilicon layer on the anti-reflective interpoly layer;
   c. a plurality of source regions adjacent to the plurality of core stacks; and
   d. a plurality of drain regions adjacent to the plurality of core stacks.

2. The flash memory device, as recited in Claim 1, wherein the plurality of source regions and the plurality of drain regions are formed by the method comprising the steps of:
   a. depositing a layer of photoresist over the substrate and the plurality of core stacks;
   b. illuminating the layer of photoresist with a light;
   c. transmitting some of the light through the transmissive second polysilicon layer;
   d. preventing the reflection of the light at the anti-reflective interpoly layer;
   e. removing part of the photoresist layer; and
   f. implanting a dopant into the substrate.

3. The flash memory device, as recited in Claim 2, wherein the light has a wavelength λ_1, and wherein the anti-reflective interpoly layer has an index of refraction n and a thickness d, and wherein the light has an integer number m wavelengths incident upon the anti-reflective interpoly layer, and wherein

$$d \cong \frac{(m+\frac{1}{2})\lambda_1}{2n}, \quad \textit{where} \quad m=0,1,2....$$

4. The flash memory device, as recited in Claim 2, wherein the light has a wavelength λ_1, and wherein the anti-reflective interpoly layer has an index of refraction n, and a thickness d, wherein

$$d \cong \frac{\lambda_1}{4n}.$$

5. The flash memory device, as recited in Claim 4, wherein the anti-reflective interpoly layer is made of silicon oxynitride (SiON).

6. The flash memory device, as recited in Claim 5, wherein the thickness of the anti-reflective interpoly layer is between about 300 to 400 Å thick.

7. The flash memory device, as recited in Claim 2, wherein the step of depositing the layer of photoresist, deposits the photoresist onto a surface of the transmissive second polysilicon layer.

8. The flash memory device, as recited in Claim 1, wherein the anti-reflective interpoly layer is made of silicon oxynitride.

9. The flash memory device, as recited in Claim 8, wherein the thickness of the anti-reflective interpoly layer is between about 300 to 400 Å thick.

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10. A method of manufacturing flash memory on a substrate, comprising the steps of: forming a plurality of core stacks on the substrate, comprising the steps of:

a. forming a tunnel oxide layer on the substrate;

b. forming a first polysilicon layer on the tunnel oxide layer;

c. forming an anti-reflective interpoly layer on the first polysilicon layer; and

d. forming a transmissive second polysilicon on the anti-reflective interpoly layer.

11. The method, as recited in Claim 10, further comprising the step of depositing a layer of photoresist over the substrate and the polysilicon layer, and wherein the photoresist reacts to a light with a wavelength λ_1, and wherein the transmissive second polysilicon transmits light with a wavelength λ_1.

12. The method, as recited in Claim 11, wherein the anti-reflective interpoly layer has an index of refraction n and a thickness d, and wherein the light has an integer number m wavelengths incident upon the anti-reflective interpoly layer, and wherein

$$d \cong \frac{(m+\frac{1}{2})\lambda_1}{2n}, \quad \textit{where} \quad m=0,1,2....$$

13. The method, as recited in Claim 11, wherein the anti-reflective interpoly layer has an index of refraction n and a thickness d, and wherein

$$d \cong \frac{\lambda_1}{4n}.$$

14. The method as recited in Claim 13, wherein the step of forming an anti-reflective interpoly layer, forms an silicon oxynitride (SiON) layer.

15. The method as recited in Claim 14, wherein the step of forming an anti-reflective layer forms the silicon oxynitride (SiON) layer to a thickness of 300 to 400 Å.

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ANTI-REFLECTIVE INTERPOLY DIELECTRIC

ABSTRACT

The invention provides core stacks for flash memory with an anti-reflective interpoly dielectric. Instead of requiring an anti-reflective coating at the top of the a stack, the present invention uses the interpoly layer as an anti-reflective coating in conjunction with a transmissive second polymer layer. Light is transmitted through the transmissive second polymer layer to the anti-reflective interpoly dielectric layer. The transmissive second polymer layer is formed from an amorphous silicon or polysilicon. Silicon oxynitride (SiON), as formed in the present invention, having a good dielectric constant K, is tailored in its index of refraction and in its thickness for utilization as both a good interpoly material and an anti-reflective coating.

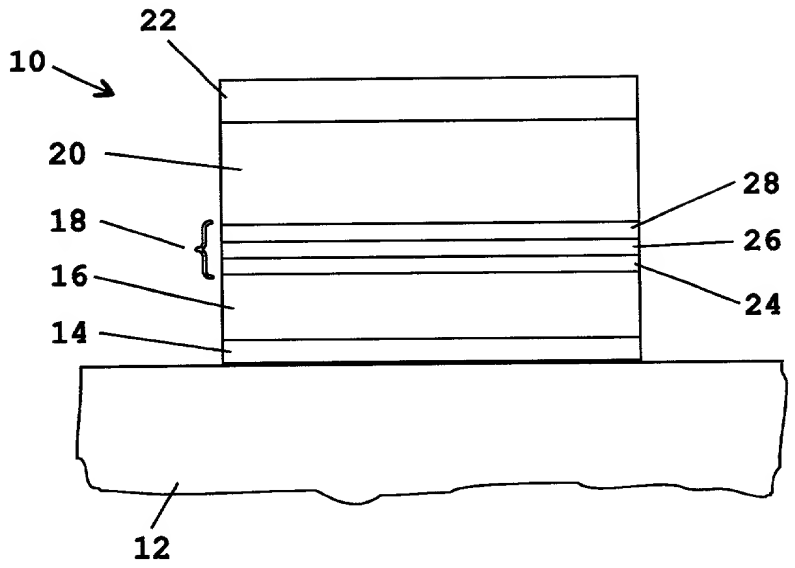

FIGURE 1 (Prior Art)

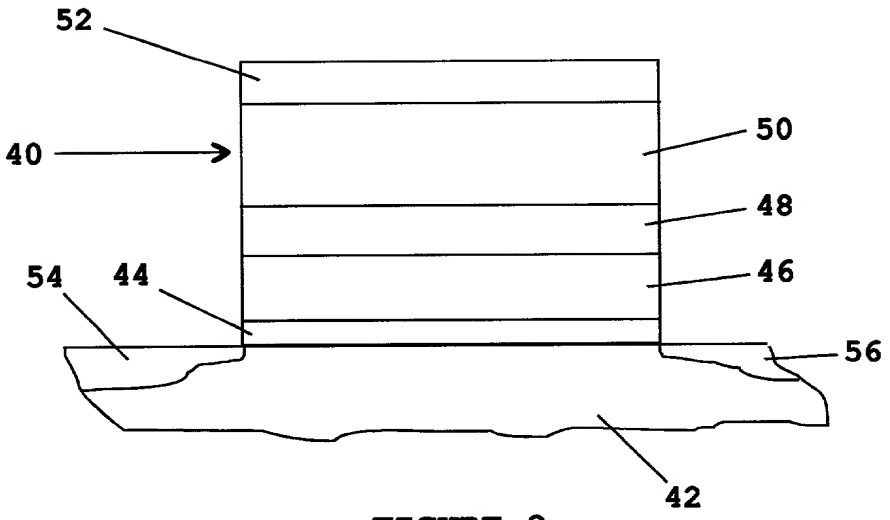

FIGURE 2

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Declaration and Power of Attorney for Patent Application

ATTORNEY'S DOCKET NO. P1057

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and jointDinventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ANTI-REFLECTIVE INTERPOLY DIELECTRIC

the specification of which ☒ is attached hereto.

☐ was filed on _____
Application Serial No._____
and was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) (Number/Country/Date Filed/Priority Claims: Yes/No)

No

I hereby claim the benefit under Title 35, United States Code, Section 120, of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a), which occurred between the filing date of the prior application and the national or PCT international filing date of this application (list application Serial No./Filing Date/Status):

Provisional Application NO. 60/179,291 01/31/2000

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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J. Vincent Tortolano Pat. Reg. No. 31,433	Vincenzo D. Pitruzzella Pat. Reg. No. 28,656	Richard J. Roddy Pat. Reg. No. 27,688	William D. Zahrt II Pat. Reg. No. 26,070
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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